IN THE CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

an insulated gate field effect transistor including

a first source/drain area of a second conductivity type formed in a semiconductor area of a first conductivity type;

a second source/drain area of the second conductivity type formed in the semiconductor area; and

a gate electrode formed on a gate insulating film on a channel area disposed between the first source/drain area and the second source/drain area, the gate insulating film includes a first gate insulating film formed on a first channel area portion and a second gate insulating film formed on a second channel area portion wherein

a second type impurity concentration distribution in the first source/drain area is different from the second type impurity concentration distribution in the second source/drain area and a thickness of the first gate insulating film is different from a thickness of the second gate insulating film.

2. The semiconductor device according to claim 1, wherein:

a first type impurity concentration distribution in the first channel area portion is different from the first type impurity concentration distribution in the

second channel area portion.

3. The semiconductor device according to claim 1, wherein:

the first gate electrode and the second gate electrode are formed in a side wall configuration.

4. The semiconductor device according to claim 1, wherein:

the first gate electrode and second gate electrode are electrically connected through a third gate electrode.

5. The semiconductor device according to claim 1, wherein:

an insulating film is formed between the first gate electrode and the second gate electrode.

6. The semiconductor device according to claim 1, wherein:

the first channel area portion is adjacent to the first source/drain area and the second channel area portion is adjacent to the second source/drain area wherein the second type impurity concentration in the first source/drain area is lower than the second type impurity concentration in the second source/drain area and the first gate insulating film is thicker than the second gate insulating film

7. The semiconductor device according to claim 1, further including:

a capacitor electrically connected to the first source/drain area; and

a bit line electrically connected to the second source/drain area wherein the second type impurity concentration in the first source/drain area is lower than the second type impurity concentration in the second source/drain area.

8. The semiconductor device according to claim 7, wherein:

the second source/drain area provides a common source/drain area for a pair of memory cells.

9. A semiconductor device, comprising:

an insulated gate field effect transistor including

a first source/drain area of a second conductivity type formed in a semiconductor area of a first conductivity type;

a second source/drain area of the second conductivity type formed in the semiconductor area; and

a gate electrode formed on a gate insulating film on a channel area disposed between the first source/drain area and the second source/drain area, the channel area including a first channel area and a second channel area, wherein

a second type impurity concentration distribution in the first source/drain area is different from the second type impurity concentration distribution in the second source/drain area and a first

type impurity concentration distribution of the first channel area is different from the first type impurity concentration distribution of the second channel area.

10. The semiconductor device according to claim 9, wherein:

the gate insulating film includes a first gate insulating film formed on the first channel area and a second gate insulating film formed on the second channel area and a thickness of the first gate insulating film is different from a thickness of the second gate insulating film; and

the first gate electrode is formed on the first gate insulating film and the second gate electrode is formed on the second gate insulating film.

11. The semiconductor device of claim 8, wherein:

the first gate electrode and the second gate electrode are formed in a side wall configuration.

12. The semiconductor device of claim 9, wherein:

the first gate electrode and second gate electrode are electrically connected through a third gate electrode.

13. The semiconductor device of claim 9, wherein:

an insulating film is formed between the first gate electrode and the second gate electrode.

14. The semiconductor device of claim 9, further including:

the first channel area is adjacent to the first source/drain area and the second channel area is adjacent to the second source/drain area wherein the second type impurity concentration in the first source/drain area is lower than the second type impurity concentration in the second source/drain area and the first type impurity concentration in the first channel area is lower than the first type impurity concentration in the second channel area.

15. The semiconductor device of claim 9, further including:

a capacitor electrically connected to the first source/drain area; and

a bit line electrically connected to the second source/drain area wherein the second type impurity concentration in the first source/drain area is lower than the second type impurity concentration in the second source/drain area.

16. A manufacturing method of a semiconductor device, the semiconductor device including a first source/drain area of a second conductivity type formed in a semiconductor area of a first conductivity type, a second source/drain area of the second conductivity type formed in the semiconductor area, a gate electrode formed on a gate insulating film on a channel area between the first source/drain area and the second source/drain area, the manufacturing method comprising the steps of:

forming a first insulating film on the semiconductor area;

forming a first mask layer at a predetermined position on the first insulating film;

forming the first source/drain area in the semiconductor area with the first mask layer;

forming a second mask layer on the first source/drain area;

forming a first channel area of the first conductivity type adjacent to the first source/drain area with the second mask layer;

forming a first gate electrode on side walls of the second mask layer;

forming a second channel area of the first conductivity type at an essentially central portion of the first channel area with the first gate electrode providing a mask;

forming a second insulating film on the second channel area, the second insulating film having a different thickness than the first insulating film;

forming a second gate electrode over the second insulating film and separated from the first gate electrode by a mediating insulating film;

forming the second source/drain area at a substantially central portion of the second channel area with the second gate electrode providing a mask; and

forming a third gate electrode providing an electrical connection for the first gate electrode and the second gate electrode.

17. The manufacturing method of a semiconductor device according to claim 16,

wherein:

a second type impurity concentration distribution of the first source/drain area is different than the second type impurity concentration distribution of the second source/drain area.

18. The manufacturing method of a semiconductor device according to claim 16, wherein:

a first type impurity concentration distribution of the first channel area is different from a first type impurity concentration distribution of the second channel area.

19. The manufacturing method of a semiconductor device according to claim 16, further including the step of:

forming a capacitor electrically connected to the first source/drain area.

20. The manufacturing method of a semiconductor device according to claim 19, wherein:

a second type impurity concentration of the first source/drain area is lower than a second type impurity concentration of the second source/drain area.